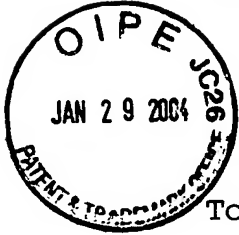


HALO-02-003



January 5, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/685,873 10/15/03 |

Seiki Ogura et al.

TWIN INSULATOR CHARGE STORAGE  
DEVICE OPERATION AND ITS FABRICATION  
METHOD

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

SB Ackerman 1/27/04

The following two articles discuss when the bottom oxide is as thin as or less than 23 Angstroms, holes are injected by a direct tunneling mechanism and the electron negative charge is neutralized by the holes:

- 1) S. Minami et al., "A Novel MONOS Nonvolatile Memory Device Ensuring 10-Year Data Retention after 10 to the 7th power Erase/Write Cycles," IEEE Trans. on Electron Device, Vol. 40, No. 11, Nov. 1993, pp. 2011-2017.
- 2) E. Suzuki et al., "Hole and Electron Current Transport in Metal-Oxide-Nitride-Oxide-Silicon Memory Structures," IEEE Trans. on Electron Device, Vol. 36, No. 6, June 1989, pp. 1145-1149.

T.Y. Chan et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device", IEEE Electron Device Letters, Vol. EDL-8, No.3, March, 1987, describes a novel single-transistor EEPROM device using single-polysilicon technology.

Kuo-Tung Chang et al., "A New SONOS Memory Using Source-Side Injection for Programming", IEEE Electron Device Letters, Vol. 19, No. 7, July, 1998, discusses a new polysilicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory using channel hot electron injection for high-speed programming.

The article by Paulo Cappelletti et al., "Flash Memories," Kluwer Academic Publishers 1999, pp. 217-223, discusses how hot hole injection is notorious for damaging oxide through injection because its effective mass is three times larger than an electron's.

U.S. Patent 6,255,166 to Ogura et al., "Nonvolatile Memory Cell, Method of Programming the Same and Nonvolatile Memory Array," provides a high speed and low program voltage nonvolatile memory cell, a programming method for same and a nonvolatile memory array.

U.S. Patent 6,469,935 to Hayashi, "Array Architecture Nonvolatile Memory and Its Operation Methods," discusses how a nonvolatile memory array architecture can be realized by a fabrication process more compatible to an MOS logic fabrication process as compared with previous nonvolatile memory array architectures.

U.S. Patent 6,531,350 to Satoh et al., "Twin MONOS Cell Fabrication Method and Array Organization," describes a fabricating method and its array organization for a high-density twin MONOS memory device integrating a twin MONOS memory cell array and CMOS logic device circuit.

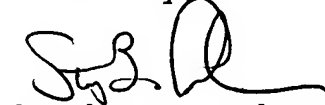
U.S. Patent 6,498,377 to Lin et al., "SONOS Component Having High Dielectric Property," describes a MONOS cell structure where nitride storage lies under sidewall spacers.

U.S. Patent 6,356,482 to Derhacobian et al., "Using Negative Gate Erase Voltage to Simultaneously Erase Two Bits from a Non-Volatile Memory Cell with an Oxide-Nitride-Oxide (ONO) Gate Structure," teaches applying a negative gate erase voltage to improve erase after many program-erase cycles.

U.S. Patent 6,040,995 to Reisinger et al., "Method of Operating a Storage Cell Arrangement," discloses F-N tunneling erase of nitride through a thick oxide layer.

U.S. Patent 5,408,115 to Chang, "Self-Aligned, Split-Gate EEPROM Device," discusses F-N tunneling erasure through the top oxide wherein the bottom oxide is thick.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman,  
Reg. No. 37761

Form PTO-1449

Docket Number (Optional)

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Applicant

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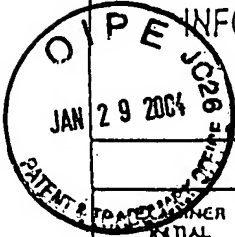
Filing Date

10/15/03

Group Art Unit

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

(Use several sheets if necessary)



U. S. PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
6255166	7/3/01	Ogura et al.	438	257	12/28/99
6469935	10/22/02	Hagashi	365	185.18	3/19/01
6531350	3/11/03	Sato et al.	438	197	11/21/01
6498377	12/24/02	Lin et al.	257	411	3/21/02
6356482	3/12/02	Derhacopian et al.	365	185.29	9/7/00
6040995	3/21/00	Reisinger et al.	365	185.18	7/29/97
5408115	4/18/95	Chang	257	324	4/4/94

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

-	S. Minami et al., "A Novel MONOS Nonvolatile Memory Device Ensuring 10-Year Data Retention after 10 <sup>7</sup> Erase/Write Cycles," <u>IEEE Trans. on Electron Device</u> , Vol. 40, No. 11, Nov. 1993, pp. 2011-2017.
-	E. Suzuki et al., "Hole and Electron Current Transport in Metal-Oxide-Nitride-Oxide-Silicon Memory Structures," <u>IEEE Trans. on Electron Device</u> , Vol. 36, No. 6, June 1989, pp. 1145-1149.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449

DocId: 34222222

Application Number

HALO-02-003

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Applicant

Seiki Ogura et al.

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## U. S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion, Pages, Etc.)

- T.Y. Chan et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device", IEEE Electron Device Letters, Vol. EDL-8, No.3, March. 1987.
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[illegible]

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-	Paulo Cappelletti et al., "Flash Memories," Kluwer Academic Publishers 1999, pp. 217-223.

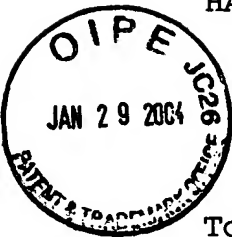
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DEVICE OPERATION AND ITS FABRICATION  
METHOD

ASSOCIATE POWER OF ATTORNEY

I hereby appoint Rosemary L.S. Pike, registration number 39,332, as my associate attorney in this case. Her telephone number is (765) 453-0866.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "SBA", followed by a large, stylized "Q" or "R" that loops around the end of the signature.

Stephen B. Ackerman,

Principal attorney of record